悠景科技股份有限公司

UG-9664HDDAG01

Application note

Evaluation Kit User Guide

Writer: Chyuan_Jyb Lin

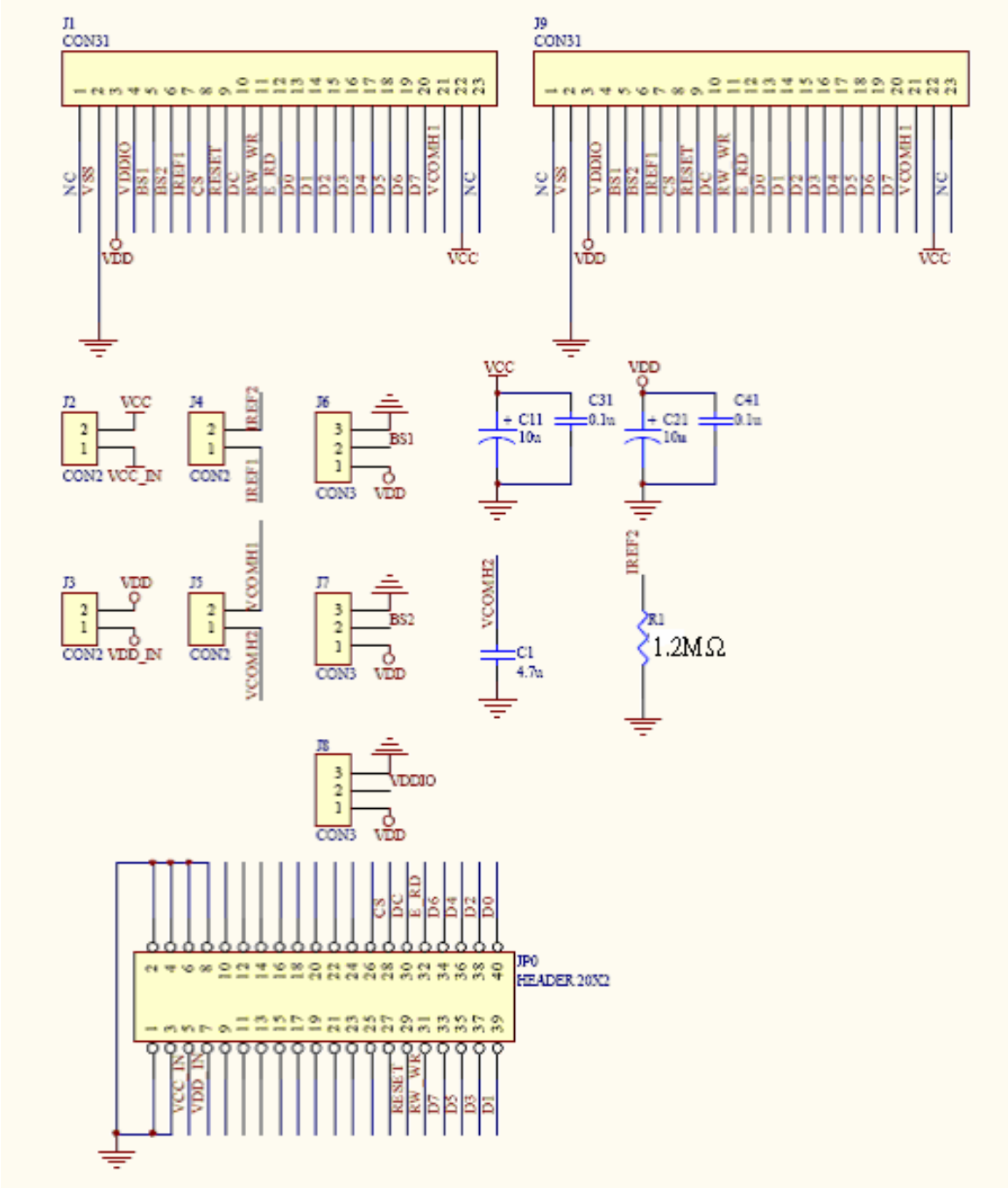
Email: Chyuan_Jyb Lin @univision.com.tw

Version: Preliminary

REVISION HISTORY

Date	Page	Contents	Version
2006/07/03	1	Preliminary	Preliminary

EVK Schematic



Symbol define

D0-D7：These pins are 8-bit bi-directional data bus to be connected to the MCU's data bus.

BS1,BS2：These input pins are used to configure MCU interface selection by appropriate logic setting, which is described in the following table. User can fixed these pins by Jump (J6, J7), or can set up by program.

	6800-parallel interface (8 bit)	8080-parallel interface (8 bit)	Serial interface
BS1	**0**	**1**	**0**
BS2	**1**	**1**	**0**

Table 1 – MCU Interface Selection Setting

E_RD：This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the chip is selected.

When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and the chip is selected. When serial interface is selected, this pin E(RD#) must be connected to VSS.

RW_WR：This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W) selection input. Read mode will be carried out when this pin is pulled high and write mode when low.

When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the chip is selected. When serial interface is selected, this pin RW_WR must be connected to VSS.

DC：This pin is Data/Command control pin. When the pin is pulled high, the data at D7-D0 is treated as display data. When the pin is pulled low, the data at D7-D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the timing characteristics diagrams.

RESET：This pin is reset signal input. When the pin is low, initialization of the chip is executed.

CS：This pin is the chip select input. The chip is enabled for MCU communication only when CS is pulled low.

VCC：This is the most positive voltage supply pin of the chip.

VDD：Power Supply pin for logic operation of the driver.

VCC_IN：This is the external most positive voltage supply. This pin should be shorted with VCC by Jump 2(J2).

VDD_IN：This is the external positive voltage supply. This pin should be shorted with VDD by Jump 3(J3).

VDDIO：Power supply for interface logic level. It should be match with the MCU interface voltage level. VDDIO must always be equal or lower than VDD (J8).

(VDD - VSS = 2.4V to 3.5V, VDDIO = 2.4V to VDD, TA = -40 to +85°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	130	-	-	ns
PW_{CSL}	Control Pulse Low Width (write cycle)	60	-	-	ns
PW_{CSH}	Control Pulse High Width (write cycle)	60	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle)	200	-	-	ns
PW_{CSL}	Control Pulse Low Width (read cycle)	100	-	-	ns
PW_{CSH}	Control Pulse High Width (read cycle)	100	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_{DSW}	Data Setup Time	40	-	-	ns
t_{DHW}	Data Hold Time	10	-	-	ns
t_{ACC}	Data Access Time	-	-	140	ns
t_{OH}	Output Hold time	-	-	70	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 2 6800-Series MPU Parallel Interface Timing Characteristics

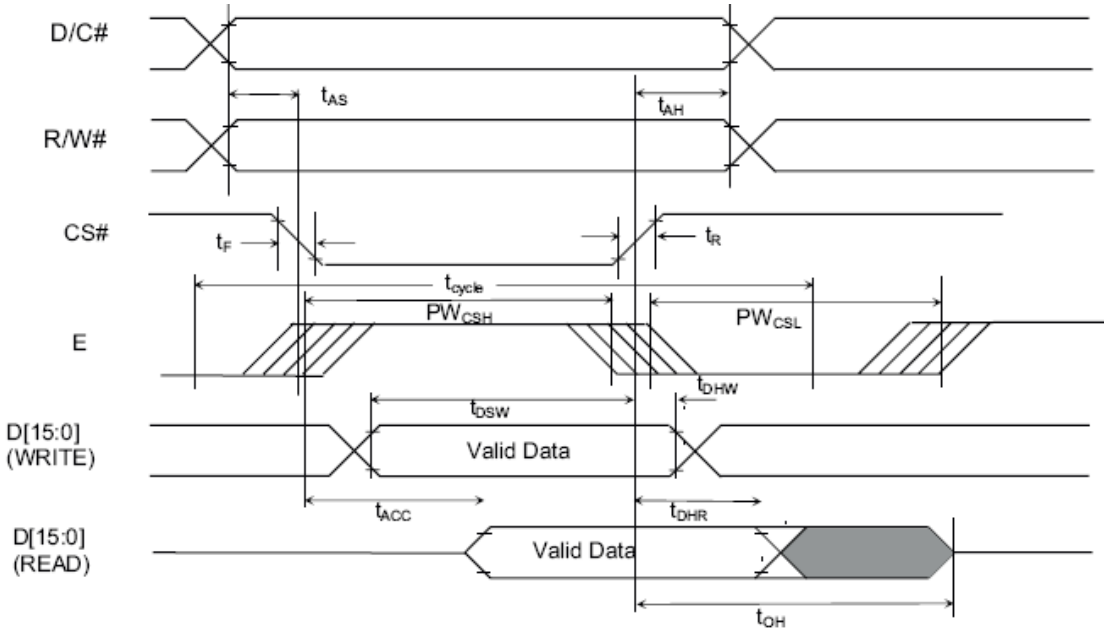


Figure 1 6800-series MPU parallel interface characteristics

(VDD - VSS = 2.4V to 3.5V, VDDIO = 2.4V to VDD, TA = -40 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	130	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	100 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 3 8080-Series MPU Parallel Interface Timing Characteristics

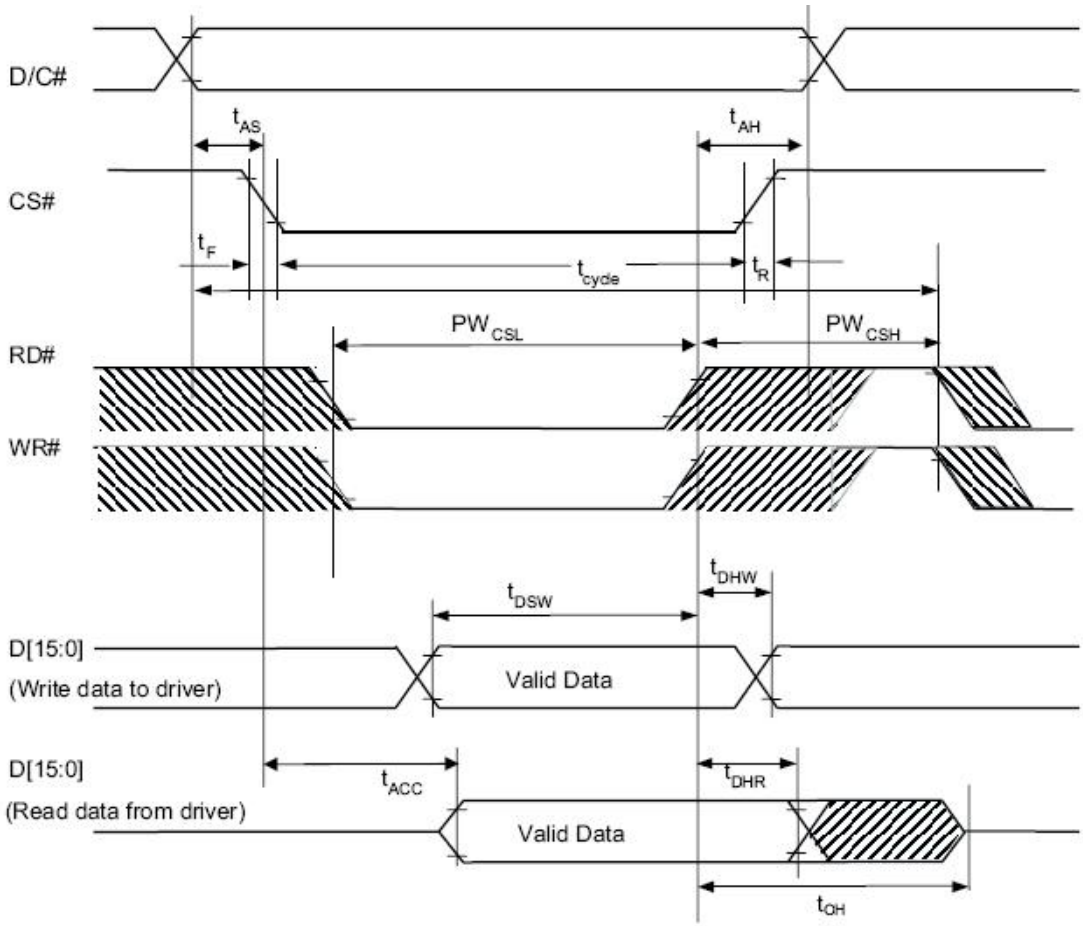


Figure 2 8080-series MPU parallel interface characteristics

(VDD - VSS = 2.4V to 3.5V, VDDIO = 2.4V to VDD, TA = -40 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	150	-	-	ns
t_{AS}	Address Setup Time	40	-	-	ns
t_{AH}	Address Hold Time	40	-	-	ns
t_{CSS}	Chip Select Setup Time	75	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	40	-	-	ns
t_{CLKL}	Clock Low Time	75	-	-	ns
t_{CLKH}	Clock High Time	75	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 4 Serial Interface Timing Characteristics

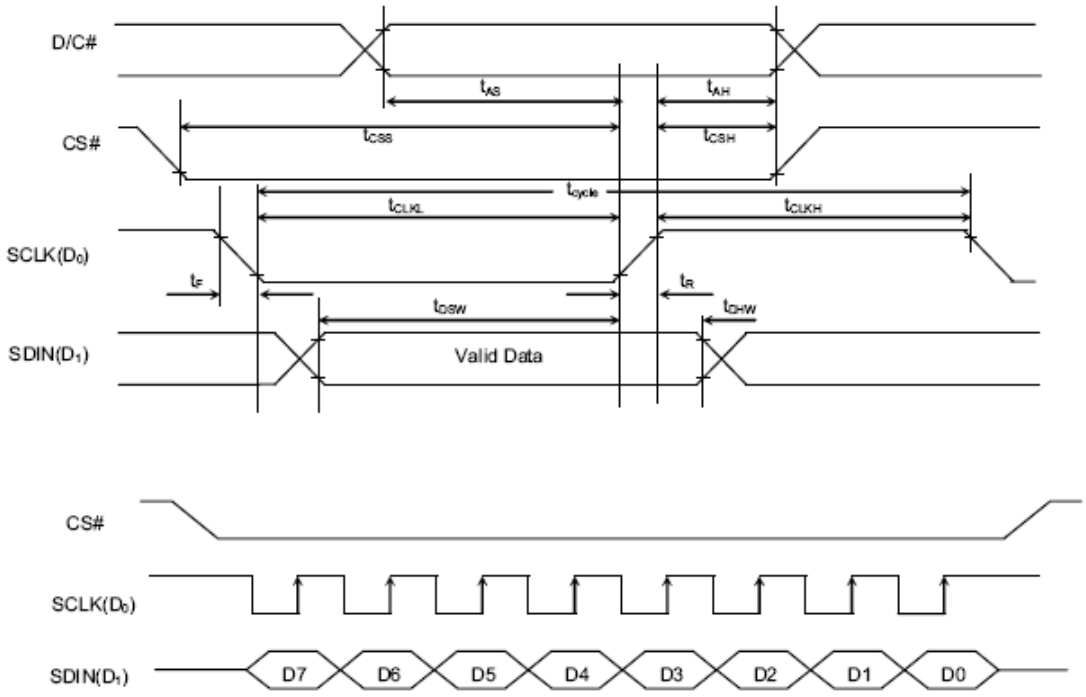


Figure 3 Serial interface characteristics

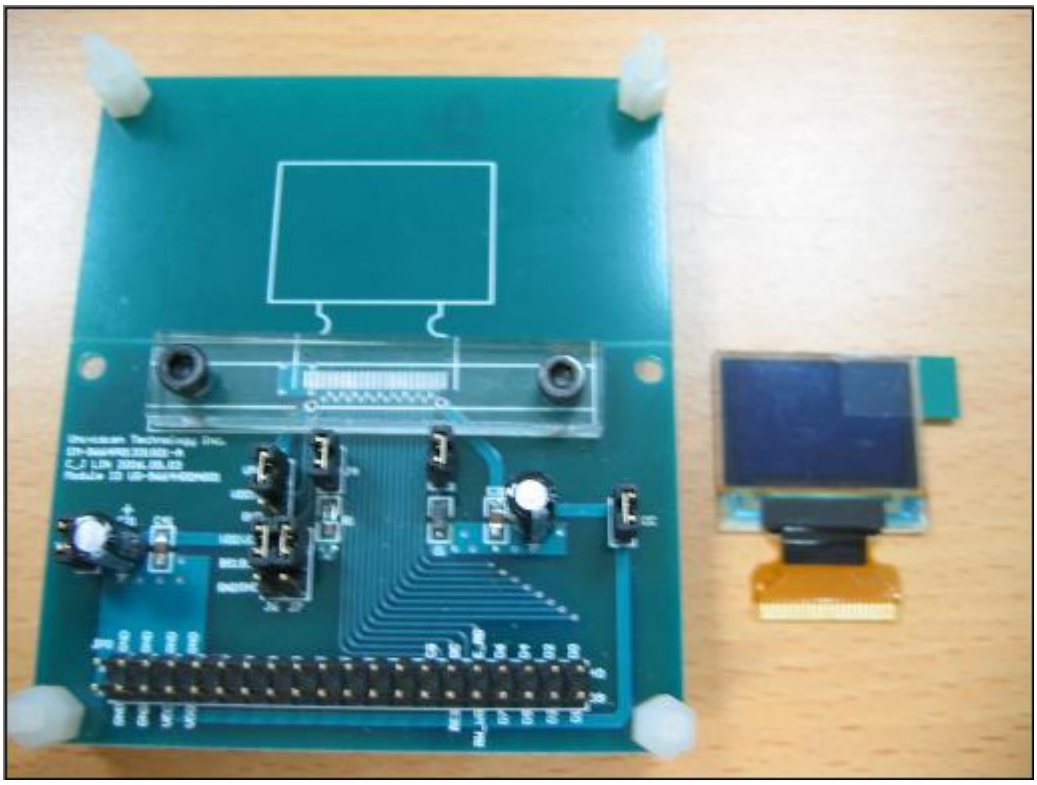


Figure 4 EVK PCB and OLED Module

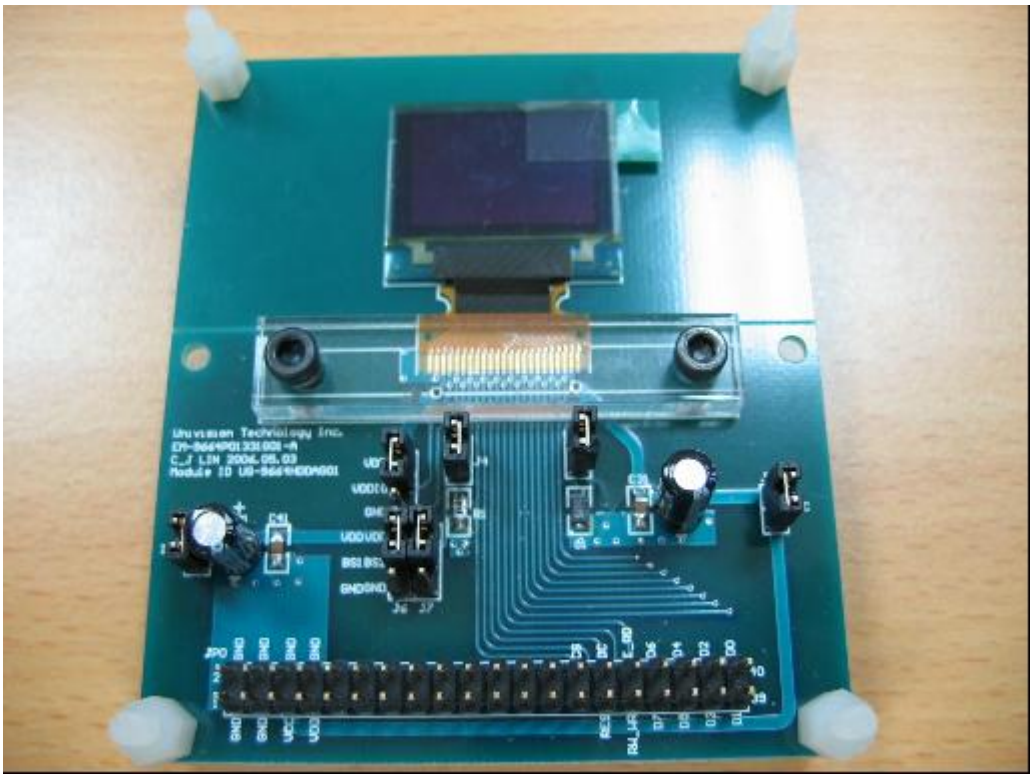


Figure 5 the module and EVK assembled (Top view)

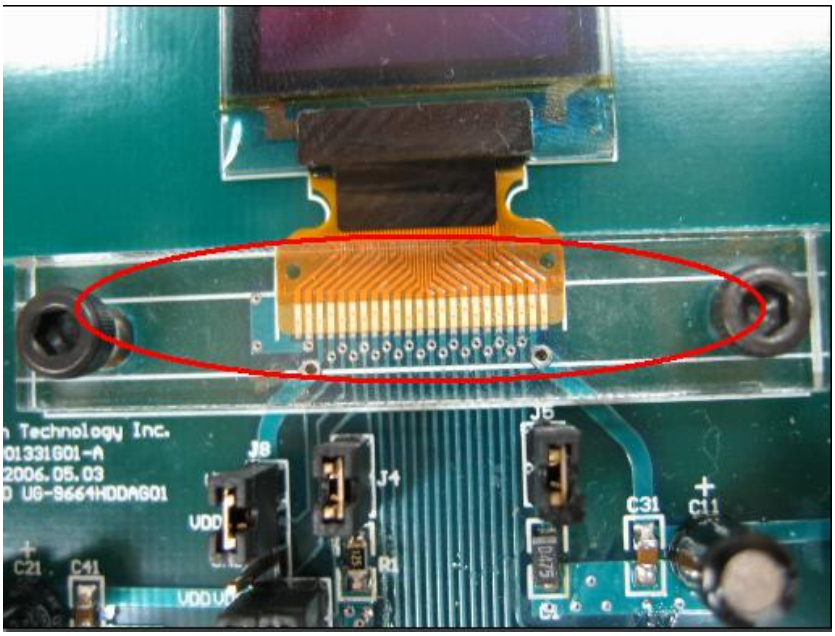


Figure 6 the module and EVK assembled (Top view)

UG-9664HDDAG01 is COG type module, please refer to Fig5, Fig6.User can use leading wire to connect EVK with customer's system. The example shows as Fig7.

.

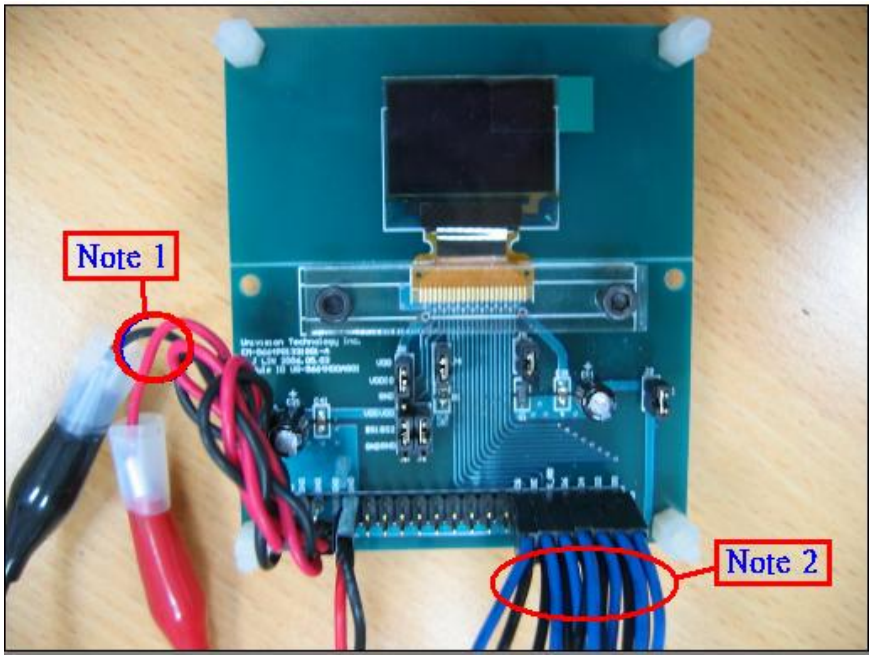


Figure 7 control MCU connect with EVK

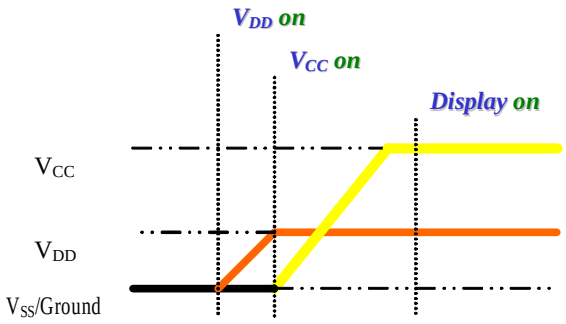
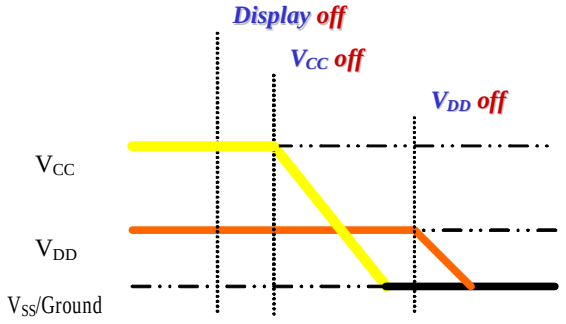
Note 1：It is the external most positive voltage supply. In this sample is connected to power supply.

Note 2：The leading wire has 13 pins totally in this case. (D0-D7,E/RD#, R/W#,E/RD#,RES#,CS#).

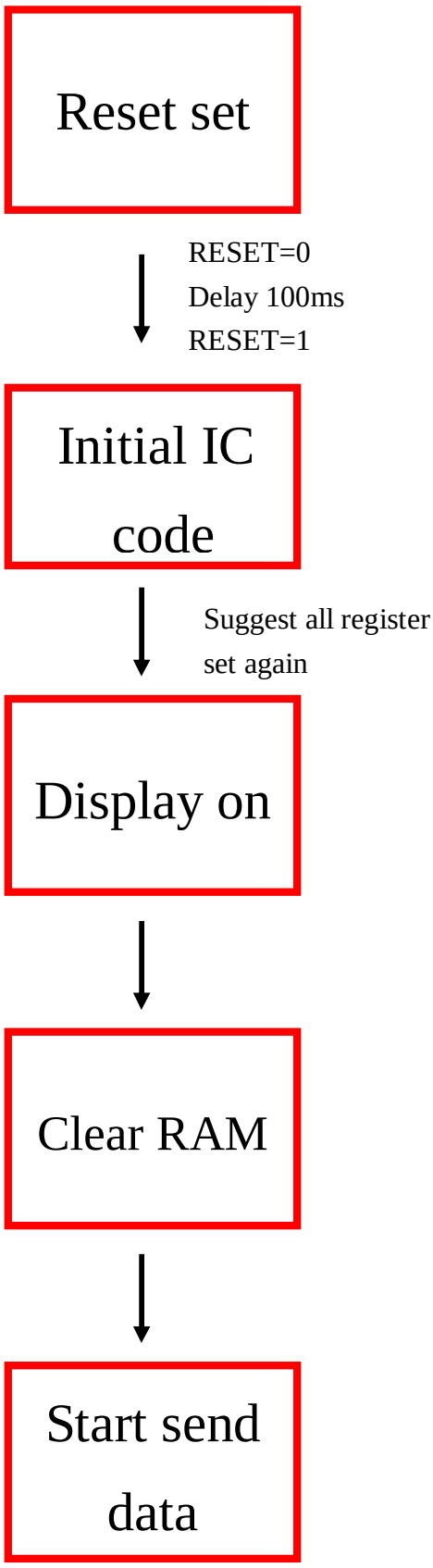
Module power on sequence

Power down and Power up Sequence

To protect OLED panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that panel has enough time to charge up or discharge before/after operation.

1.1 Power up Sequence: 1. Power up V_{DD} 2. Send Display off command 3. Driver IC Initial Setting 4. Clear Screen 5. Power up V_{DDH} 6. Delay 100ms (when V_{DD} is stable) 7. Send Display on command	
1.2 Power down Sequence: 1. Send Display off command 2. Power down V_{DDH} 3. Delay 100ms (when V_{DDH} is reach 0 and panel is completely discharges) 4. Power down V_{DD}	

How to use UG-9664HDDAG01 module



Initial setting suggest：

```
Void Initial_ic(void)
{
    IOCLR=0xffffffff;        //data=0
    IOSET=bBS1|bBS2|bRES|bCS|bE_RD;
    IOCLR=bD_C|bR_W;
    Reset_SSD1331Z();
    Write_Register (0xae);            //Display off

    Write_Register(0x81);             //set contrast for colorA
    Write_Register(0x91);             //145

    Write_Register(0x82);             //set contrast for colorB
    Write_Register(0x50);             //80

    Write_Register(0x83);             //set contrast for colorC
    Write_Register(0x7d);             //125

    Write_Register(0x87);             //master current control
    Write_Register(0x06);             //6

    Write_Register(0x8a);             //Set Second Pre-change Speed For ColorA
    Write_Register(0x64);             //100
    Write_Register(0x8b);             //Set Second Pre-change Speed For ColorB
    Write_Register(0x78);             //120
    Write_Register(0x8c);             //Set Second Pre-change Speed For ColorC
    Write_Register(0x64);             //100

    Write_Register(0xa0);             //set re=map & data format
    Write_Register(0x74);

    Write_Register(0xa1);             //set display start line
    Write_Register(0x00);

    Write_Register(0xa2);             //set display offset
    Write_Register(0x00);
```

```
        Write_Register(0xa4);           //set display mode

        Write_Register(0xa8);           //set multiplex ratio
        Write_Register(0x3f);

        Write_Register(0xad);           //set master configuration
        Write_Register(0x8e);

        Write_Register(0xb0);           //set power save
        Write_Register(0x00);

        Write_Register(0xb1);           //phase 1 and 2 period adjustment
        Write_Register(0x31);

        Write_Register(0xb3);           //display clock divider / oscillator frequency
        Write_Register(0xf0);

        Write_Register(0xbb);           //Set Pre-Change Level
        Write_Register(0x3a);           //58

        Write_Register(0xbe);           //set vcomh
        Write_Register(0x3e);           //62

        Write_Register(0xaf);           //set display on}

void Reset_SSD1331Z(void)
{
        IOCLR=bRES;
        Delay_1ms(10);
        IOSET=bRES;

void Write_Register (unsigned char out_command)
{
        IOCLR=bD_C;
        IOCLR=bCS;
        IOCLR=bR_W;
        IOCLR=0x000000ff;
        IOSET= out_command;
        IOSET=bR_W;
        IOSET=bCS;
}

void Write_Data (unsigned char out_data)
{
        IOSET=bD_C;
        IOCLR=bCS;
```

```
        IOCLR=bR_W;
        IOCLR=0x000000ff;
        IOSET=out_data;
        IOSETbR_W;
        IOSET=bCS;
}

void Delay_1ms(int Cycle)
{
unsigned int i,k;
        for (i=0 ;i<Cycle;i++)
                for(k=0;k<0x2fff;k++);
}
```